REMARKS

This Amendment is filed in response to the final Office Action dated August 2, 2004, which has a shortened statutory period set to expire November 2, 2004.

Clarification Requested Regarding Claim Rejections

The final Office Action indicates that Claims 37-53 and 55-58 are rejected as being obvious over Beausang in view of Testing. In the actual rejection of Claims 37-47, 49, 51-53, and 55-58 only Beausang is cited. For completeness of response, Applicants have indicated the patentability of each of the claims based on Beausang as well as Testing. However, should an appeal be necessary, Applicants request clarification of the rejections of Claims 37-47, 49, 51-53, and 55-58.

The Combination Of Beausang and Testing Is Inappropriate

Beausang teaches a computer implemented process and system for determining a set of sequential cells within an IC design that can be scan replaced. Col. 4, lines 57-59. Specifically, Beausang teaches selecting sequential cells for scan replacement that offer best testability contribution and not selecting sequential scan cells for scan replacement that do not offer much testability contribution and/or are part of most critical paths within the design. Col. 4, lines 59-67.

Testing teaches how to use design particularities (such as bus keepers and resolving bus contention states to binary values) with transistor-level modeling and innovative use of ATPG methods to address test generation performance and test coverage problems generated by the extensive usage of tristate circuitry. Page 330-331 (Section 7. Summary).

Notably, the teaching of Testing does not help in determining the set of sequential cells within an IC design that

can be scan replaced (Beausang). Nor does the teaching of Beausang help in determining an ATPG method to address test generation performance and test coverage problems generated by the use of tristate circuitry (Testing). In short, Beausang and Testing address different problems and resolve these problems in different ways.

Therefore, Applicants submit that Beausang and Testing are improperly combined. For completeness of response, Applicants now present reasons why, even if Beausang and Testing are combinable, the claims are neither disclosed nor suggested by this cited art.

Claim 37 Is Patentable Over The Cited References

Claim 37 recites:

> A memory model usable for simulation and automatic test pattern generation, the memory model comprising:
>
> a memory primitive comprising a write_address port, a write_data port, and an output port;
>
> a read data port primitive comprising a read_data port for coupling to the output port of the memory primitive, a read_address port, and an output port;
>
> an address bus primitive comprising an output port for coupling to the write_address port of the memory primitive and the read_address port of the read data port primitive;
>
> a data bus primitive comprising an output port for coupling to the write_data port of the memory primitive; and
>
> a plurality of memory out primitives, each memory out primitive comprising an input port for coupling to the output port of the read data port primitive.

The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of

Claim 37. Applicants will now address the inapplicability of each citation to Claim 37.

Col. 1, lines 53-67 of Beausang states:

> The components of a netlist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates, latches, and D- flip flops, etc. and their interconnections used to form a custom design.
>
> In processing the HDL input, the compiler first generates a netlist of generic primitive cells that are technology independent. The compiler then applies a particular cell library to this generic netlist (this process is called mapping) in order to generate a technology dependent mapped netlist. The mapping process converts the logical representation which is independent of technology into a form which is technology dependent. The mapped netlist has recourse to standard circuits, or cells which are available within a cell library forming a part of the data available to the computer system.

This citation of Beausang teaches nothing regarding the memory model recited in Claim 37. Specifically, the above citation to Beausang teaches nothing regarding a memory primitive comprising a write_address port, a write_data port, and an output port, nor a read data port primitive comprising a read_data port for coupling to the output port of the memory primitive, a read_address port, and an output port, nor an address bus primitive comprising an output port for coupling to the write_address port of the memory primitive and the read_address port of the read data port primitive, nor a data bus primitive comprising an output port for coupling to the write_data port of the memory primitive, nor a plurality of memory out primitives, each memory out primitive comprising an input port for coupling to the output port of the read data port primitive. Beausang's generalized statement regarding primitive cells does not disclose the primitives recited by Applicants.

Moreover, the primitives of Beausang are used to model logic, not memory as recited by Applicants.

In short, col. 1, lines 53-67 of Beausang fails to teach any limitation of Claim 37. Applicants further note the characterization in the Office Action that "latches and D-flip flops" disclose memory primitives is incorrect and not supported. Additionally, the characterization in the Office Action that "and their interconnections" discloses the address bus and data bus is incorrect and not supported.

Col. 14, lines 39-42 (providing the context for line 40) of Beausang states:

> Technology independent netlist 620 is composed of logical primitives and operators of the IC layout but the components described therein contain no structure.

This citation fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Element 230 of Fig. 1 in Beausang refers to a technology dependent cell library. Col. 2, line 50. Cell library 230 contains specific information selected such as the cell logic, number of gates, area consumption, power consumption, pin descriptions, etc., for each cell in the library 230. Col. 2, lines 51-55. Element 230 fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Elements 605 of Fig. 8 in Beausang refers to an HDL description that can be of a number of different formats, such as VHDL or Verilog and can also represent an entire IC design, but typically represents a module of the overall IC design. Col. 14, lines 27-30. Element 605 fails to teach anything regarding the memory model recited in Claim 37, much less the

recited primitives comprising the memory model and their interconnections.

Element 660 of Fig. 8 in Beausang refers to test vectors that can be loaded into the result IC chip to check for faults within the chip. Col. 16, lines 26-28. Element 660 fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Element 790 of Fig. 9 in Beausang refers to a logic block in which the TR compiler 625 performs logic verification to determine if the design generated by logic block 785 and the HDL design input at logic block 710 are functionally equivalent. Col. 20, lines 3-6. Element 790 fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Testing fails to remedy the deficiency of Beausang. Specifically, Testing fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections. Applicants note that the bus discussed in Testing refers to a multiplely driven net, whereas the recited bus refers to set of nets (not multiplely driven) that belong together.

Because neither Beausang nor Testing disclose or suggest the recited limitations of Claim 37, Applicants request reconsideration and withdrawal of the rejection of Claim 37.

Claim 38 Is Patentable Over The Cited References

Claim 38 recites:

> The memory model of Claim 37, wherein the memory primitive further includes:
> a set input port;

a reset port;
a write_clock port; and
a write_enable port.

Claim 38 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 38 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 38 recites further limitations regarding the memory primitive. Because neither Beausang nor Testing discloses a memory primitive, they logically cannot disclose the ports of that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 38.

Claim 39 Is Patentable Over The Cited References

Claim 39 recites:

> The memory model of Claim 37, wherein the read data port primitive represents a read port functionality of the memory.

Claim 39 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 39 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 39 recites further limitations regarding the read data port primitive. Because neither Beausang nor Testing discloses a read data port primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore,

Applicants request reconsideration and withdrawal of the rejection of Claim 39.

Claim 40 Is Patentable Over The Cited References

Claim 40 recites:

> The memory model of Claim 39, wherein a dimension of the output port of the read data port corresponds to a data dimension of the memory primitive.

Claim 40 depends from Claim 39 and therefore is patentable for at least the reasons presented for Claim 39. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 40 (the same citations used for Claim 37). Because neither Beausang nor Testing discloses a read data port, they logically cannot disclose a further limitation regarding that port. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 40.

Claim 41 Is Patentable Over The Cited References

Claim 41 recites:

> The memory model of Claim 37, wherein the address bus primitive represents an address functionality of a memory.

Claim 41 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 41 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37.

Claim 41 recites a further limitation regarding the address bus primitive. Because neither Beausang nor Testing discloses a address bus primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 41.

Claim 42 Is Patentable Over The Cited References

Claim 42 recites:

> The memory model of Claim 41, wherein the address bus primitive includes:
> a plurality of input ports corresponding to an address dimension of the memory primitive.

Claim 42 depends from Claim 41 and therefore is patentable for at least the reasons presented for Claim 41. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 42 (the same citations used for Claim 37). Because neither Beausang nor Testing discloses an address bus primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 42.

Claim 43 Is Patentable Over The Cited References

Claim 43 recites:

> The memory model of Claim 42, wherein the address bus primitive further includes an attribute indicating whether an incoming address is encoded or decoded.

Claim 43 depends from Claim 42 and therefore is patentable for at least the reasons presented for Claim 42. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40,

element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 38 (the same citations used for Claim 37). Because neither Beausang nor Testing discloses a address bus primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 43.

Claim 44 Is Patentable Over The Cited References

Claim 44 recites:

> The memory model of Claim 43, wherein the data bus primitive represents a data bus functionality of the memory.

Claim 44 depends from Claim 43 and therefore is patentable for at least the reasons presented for Claim 43. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 44 (the same citations used for Claim 37). Because neither Beausang nor Testing discloses a data bus primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 44.

Claim 45 Is Patentable Over The Cited References

Claim 45 recites:

> The memory model of Claim 44, wherein the data bus includes:
> a plurality of input ports corresponding to a data dimension of the memory primitive.

Claim 45 depends from Claim 44 and therefore is patentable for at least the reasons presented for Claim 44. The Office

Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 45 (the same citations used for Claim 37). Because neither Beausang nor Testing discloses a data bus primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 45.

Claim 46 Is Patentable Over The Cited References

Claim 46 recites:

> The memory model of Claim 37, wherein each memory out primitive represents a simulated value storage functionality of the memory.

Claim 46 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 46 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 46 recites a further limitation regarding the memory out primitive. Because neither Beausang nor Testing discloses a memory out primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 46.

Claim 47 Is Patentable Over The Cited References

Claim 47 recites:

> The memory model of Claim 37, wherein each memory out primitive includes an output port.

Claim 47 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 47 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 47 recites a further limitation regarding the memory out primitive. Because neither Beausang nor Testing discloses a memory out primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 47.

Claim 48 Is Patentable Over The Cited References

Claim 48 recites:

> The memory model of Claim 47, wherein a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

Claim 48 depends from Claim 47 and therefore is patentable for at least the reasons presented for Claim 47. The Office Action cites Testing as disclosing the elements of Claim 48. Because neither Beausang nor Testing discloses a memory out primitive or a read data port primitive, they logically cannot disclose a further limitation regarding that a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 48.

Claim 49 Is Patentable Over The Cited References

Claim 49 recites:

> The memory model of Claim 47, wherein a plurality of edge-triggered registers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

Claim 49 depends from Claim 47 and therefore is patentable for at least the reasons presented for Claim 47. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 38 (the same citations used for Claim 37). Because neither Beausang nor Testing discloses a memory out primitive or a read data port primitive, they logically cannot disclose a further limitation that a plurality of edge-triggered registers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 49.

Claim 50 Is Patentable Over The Cited References

Claim 50 recites:

> The memory model of Claim 49, wherein input ports of a plurality of tristate drivers can be coupled to output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive.

Claim 50 depends from Claim 49 and therefore is patentable for at least the reasons presented for Claim 49. The Office Action cites Testing as disclosing the elements of Claim 50. Because neither Beausang nor Testing discloses a read data port primitive, they logically cannot disclose a further limitation

that a plurality of tristate drivers can be coupled to the output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 50.

Claim 51 Is Patentable Over The Cited References

Claim 51 recites:

> A content addressable memory model usable for simulation and automatic test pattern generation, the content addressable memory model comprising:
>
> a memory primitive including an output port;
>
> a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port;
>
> a data bus primitive including an output port for coupling to the data bus port of the compare port primitive;
>
> a plurality of memory output primitives, each memory output primitive including an input port for coupling to the output port of the compare port primitive and an output port; and
>
> an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives.

The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 37. Applicants will now address the inapplicability of each citation to Claim 51.

Col. 1, lines 53-67 of Beausang states:

> The components of a netlist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates, latches, and D- flip flops, etc. and their interconnections used to form a custom design.

> In processing the HDL input, the compiler first generates a netlist of generic primitive cells that are technology independent. The compiler then applies a particular cell library to this generic netlist (this process is called mapping) in order to generate a technology dependent mapped netlist. The mapping process converts the logical representation which is independent of technology into a form which is technology dependent. The mapped netlist has recourse to standard circuits, or cells which are available within a cell library forming a part of the data available to the computer system.

This citation of Beausang teaches nothing regarding the content addressable memory model recited in Claim 51. Specifically, the above citation to Beausang teaches nothing regarding a memory primitive including an output port, nor a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port, nor a data bus primitive including an output port for coupling to the data bus port of the compare port primitive, nor a plurality of memory output primitives, each memory output primitive including an input port for coupling to the output port of the compare port primitive and an output port, nor an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives. In short, col. 1, lines 53-67 of Beausang fails to teach any limitation of Claim 51. Beausang's generalized statement regarding primitive cells does not disclose the primitives recited by Applicants. Moreover, the primitives of Beausang are used to model logic, not memory as recited by Applicants.

Col. 14, lines 39-42 (providing the context for line 40) of Beausang states:

> Technology independent netlist 620 is composed of logical primitives and operators of

> the IC layout but the components described therein contain no structure.

This citation fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Element 230 of Fig. 1 in Beausang refers to a technology dependent cell library. Col. 2, line 50. Cell library 230 contains specific information selected such as the cell logic, number of gates, area consumption, power consumption, pin descriptions, etc., for each cell in the library 230. Col. 2, lines 51-55. Element 230 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Elements 605 of Fig. 8 in Beausang refers to an HDL description that can be of a number of different formats, such as VHDL or Verilog and can also represent an entire IC design, but typically represents a module of the overall IC design. Col. 14, lines 27-30. Element 605 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Element 660 of Fig. 8 in Beausang refers to test vectors that can be loaded into the result IC chip to check for faults within the chip. Col. 16, lines 26-28. Element 660 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Element 790 of Fig. 9 in Beausang refers to a logic block in which the TR compiler 625 performs logic verification to determine if the design generated by logic block 785 and the HDL

design input at logic block 710 are functionally equivalent. Col. 20, lines 3-6. Element 790 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Testing fails to remedy the deficiency of Beausang. Specifically, Testing fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Because neither Beausang nor Testing disclose or suggest the recited limitations of Claim 51, Applicants request reconsideration and withdrawal of the rejection of Claim 51.

Claim 52 Is Patentable Over The Cited References

Claim 52 recites:

> The content addressable memory model of Claim 51, wherein the compare port primitive further includes:
>
> a compare enable port for receiving a compare signal.

Claim 52 depends from Claim 51 and therefore is patentable for at least the reasons presented for Claim 51. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 52 (the same citations used for Claim 51). Applicants have addressed the inapplicability of each citation to Claim 51. Claim 52 recites a further limitation regarding the compare port primitive. Because neither Beausang nor Testing discloses a compare port primitive, they logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants

request reconsideration and withdrawal of the rejection of Claim 52.

Claim 53 Is Patentable Over The Cited References

Claim 53 recites:

> A combined content addressable memory (CAM) and random access memory (RAM) model usable for simulation and automatic test pattern generation, the combined CAM and RAM model comprising:
> a first memory primitive including an output port;
> a data bus primitive including an output port;
> a compare port primitive for coupling to the memory primitive and the data bus primitive, the compare port primitive comprising;
> a compare enable port;
> a data bus port for coupling to the output port of the data bus primitive;
> a data port for coupling to the output port of the first memory primitive; and
> an output port;
> a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive;
> an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives;
> a second memory primitive including an output port;
> a read data port primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives; and
> a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive.

The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 53. Applicants will now address the inapplicability of each citation to Claim 53.

Col. 1, lines 53-67 of Beausang states:

> The components of a netlist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates, latches, and D- flip flops, etc. and their interconnections used to form a custom design.
>
> In processing the HDL input, the compiler first generates a netlist of generic primitive cells that are technology independent. The compiler then applies a particular cell library to this generic netlist (this process is called mapping) in order to generate a technology dependent mapped netlist. The mapping process converts the logical representation which is independent of technology into a form which is technology dependent. The mapped netlist has recourse to standard circuits, or cells which are available within a cell library forming a part of the data available to the computer system.

This citation of Beausang teaches nothing regarding the combined CAM and RAM model recited in Claim 53. Specifically, the above citation to Beausang teaches nothing regarding a first memory primitive including an output port, nor a data bus primitive including an output port, nor a compare port primitive for coupling to the memory primitive and the data bus primitive, nor a compare port primitive comprising a compare enable port, a data bus port for coupling to the output port of the data bus primitive, a data port for coupling to the output port of the first memory primitive, and an output port, nor a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive, nor

an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives, nor a second memory primitive including an output port, nor a read data port primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives, nor a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive. In short, col. 1, lines 53-67 of Beausang fails to teach any limitation of Claim 53. Beausang's generalized statement regarding primitive cells does not disclose the primitives recited by Applicants. Moreover, the primitives of Beausang are used to model logic, not memory as recited by Applicants.

Col. 14, lines 39-42 (providing the context for line 40) of Beausang states:

> Technology independent netlist 620 is composed of logical primitives and operators of the IC layout but the components described therein contain no structure.

This citation fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Element 230 of Fig. 1 in Beausang refers to a technology dependent cell library. Col. 2, line 50. Cell library 230 contains specific information selected such as the cell logic, number of gates, area consumption, power consumption, pin descriptions, etc., for each cell in the library 230. Col. 2, lines 51-55. Element 230 fails to teach anything regarding the

combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Elements 605 of Fig. 8 in Beausang refers to an HDL description that can be of a number of different formats, such as VHDL or Verilog and can also represent an entire IC design, but typically represents a module of the overall IC design. Col. 14, lines 27-30. Element 605 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Element 660 of Fig. 8 in Beausang refers to test vectors that can be loaded into the result IC chip to check for faults within the chip. Col. 16, lines 26-28. Element 660 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Element 790 of Fig. 9 in Beausang refers to a logic block in which the TR compiler 625 performs logic verification to determine if the design generated by logic block 785 and the HDL design input at logic block 710 are functionally equivalent. Col. 20, lines 3-6. Element 790 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Testing fails to remedy the deficiency of Beausang. Specifically, Testing fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Because neither Beausang nor Testing disclose or suggest the recited limitations of Claim 53, Applicants request reconsideration and withdrawal of the rejection of Claim 53.

Claim 55 Is Patentable Over The Cited References

Claim 55 recites:

> A memory model compatible with a simulation tool and an automatic test pattern generation (ATPG) tool, the memory model including:
> a plurality of primitives, each primitive representing a defined functionality of a memory.

The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 55. Applicants submit that Claim 55 is patentable for substantially the same reasons presented above for Claim 37. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 55.

Claims 56, 57, and 58 Are Patentable Over The Cited References

Claim 56 depends from Claim 55 and therefore is patentable for at least the reasons presented for Claim 55. Claims 57 and 58 depend from Claim 56 and therefore are patentable for at least the reasons presented for Claim 56. Based on all of the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 56, 57, and 58.

CONCLUSION

Claims 37-53 and 55-58 are pending in the present application. Applicants request allowance of these claims.

If the next action is other than allowance, please telephone the undersigned at 408-451-5907 to schedule a telephone interview.

Respectfully submitted,

Customer No.: 35273

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 27, 2004.

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